Techniques for Forming Simplified Computational Models for Circuit Simulation

Sergey G. Rusakov

Research Institute of CAD Systems of VLSI
Academy of Sciences of Russia
Moscow 105023, Russia

Abstract

Two formalized approaches to reducing the model computational complexity for improving the efficiency of circuit simulation are presented. The possibility to decrease computational complexity of well-known model equations due to application of special functions is described. The technique for forming nonlinear dynamical macromodel from original component-level model of subcircuit block is proposed. This approach may be introduced as a basic computational procedure for solving the problem of automatic generation of macromodels.

1 Introduction

Macromodeling is one of the main direction of computational complexity reducing in electrical simulation of VLSI circuits [1-7]. At the present time various general and special-purpose macromodels (MM) have been developed and they are successfully used in the circuit design, including analog circuits (for example, [2,5]) or digital circuits (for example, [3,4]). The problem of automatic generation of MM [6,7,9,10] has become actual today. Its solution requires the presence of formalized computational procedures for MM construction.

It is more expedient to carry out the investigations on the automatic generation MM algorithms in the class of methods for obtaining the simplified subcircuit models from their full mathematical models [10]. Such algorithms allow to take into account the a priory information about original subcircuit on transistor level. The principal mathematical problems in this case are connected with the forming of the dynamical MM for the nonlinear version. The initial complete subcircuit block model is given by set of equations:

$$\begin{aligned} f\ (\dot{x},\ x,\ \dot{y},\ y,\ P) &= 0 \\ I_T &= h\ (\dot{x},\ x,\ \dot{y},\ y,\ P) \end{aligned} \qquad (1)$$

Here x(t) and y(t) - vector-functions of the internal and external circuit variables , P - vector of the circuit parameters. In case of the nodal analysis I_T is vector of subcircuit terminal currents.

The problem of construction of subcircuit block MM supposes reducing this model order, in particular the elimination of internal variables x.

One can classify three approaches to solve the problem of reducing initial model order:

- the numerical experiments with complete model (1) for the following identification of MM with the account of calculated external characteristics (for example, [7]);
- simplification of original complete model on the transistor level;
- formalized transformation of complete model (1) to low-order model.

From the view point of automation we consider the third approach more perspective.

Section 2 describes the developed macromodeling approach. This technique implements the ideas of perturbation method (for example, [8]) for synthesis of low-frequency models. It gives possibilities to lead the generation of dynamical MM to static problem. The obtained formulas can be used in the systems for automatic generation of MM.

The purpose of section 3 is to show, that significant resources for saving computational efforts are presented in using rational mathematical description of well-known models, in particular the models of diode and bipolar transistor with series resistances. The quite general approach to increase computational efficiency of calculation of model characteristic by saving initial precision is given. The approach is based on implementation of a single description of the processes with two concurrent mechanisms by the special function.

2 Macromodeling technique approach

Our purpose is a generation of time-domain MM from complete subcircuit model (1) in the following form:

$$I_M = g_{ST} + C_{EQ} * \dot{y} , \qquad (2)$$

where g_{ST} - static macromodel characteristics and C_{EQ} - the matrix of the equivalent capacitances.

Let us consider that the static solution of the set (1) is known

$$f(0,\ x,\ 0,\ y) = 0 \tag{3}$$

for different values of vector y, i.e. function $x_{ST}(y)$ is determined. Then we introduce the solution of (1) in the following form:

$$x(t) = x_{ST}(y(t)) + \delta x(t) \tag{4}$$

where x(t) - deviation from static solution. The main assumption of discussed technique is the following:

$$\delta\dot{x}(t) << \dot{x}_{ST}(t) \tag{5}$$

i.e. the own inertia of the internal nodes is essentially lower than the terminal nodes inertia. Such condition is right in many practical cases. It can be noticed, that if condition (5) is wrong for any nodes then in frames of proposed methodology these nodes can be formally classified as terminal. We can determine $\dot{x}(t)$ by differentiation the equation (4) as compound function taking into account condition (5). Then the set (1) can be rewritten in following form:

$$f(x_{ST}(y) + \delta x,\ (\partial x_{ST}/\partial y)*\dot{y},\ y,\ \dot{y}) = 0 \tag{6}$$

$$I_T = h(x_{ST}(y) + \delta x,\ (\partial x_{ST}/\partial y)*\dot{y},\ y,\ \dot{y}) \tag{7}$$

The resulting form of MM (2) can be got by obtaining x(y,y) from (6) and substituting this function to equation (7). To define the formulae for transforming initial capacitances matrices to equivalent matrix (2) we take into account the independence of the capacitances from the derivatives and carry out linearization of equations (6) and (7) relatively x. In this case we can get for MM form (2) the following formulae of calculating the matrix of terminal capacitances.

$$C_{EQ} = [\partial h/\partial\dot{y} + \partial h/\partial\dot{x} * dx/dy] - \partial h/\partial x * (\partial f/\partial x)^{-1}[\partial f/\partial\dot{y} + \partial f/\partial\dot{x} * dx/\partial y] \tag{8}$$

The example of transformation RC-network to equivalent circuit (fig.1) illustrates the peculiarities of using formulae (8).
The proposed approach allows to obtain the low-frequency MM. The following equation is the condition of its application:

$$w*||(\partial f/\partial x)^{-1}*\partial f/\partial \dot{x}||<1$$

where w - cyclic frequency. The estimation of dynamical error of formulae (8) can be also obtained:

$$||O(w^2)||=\frac{\partial h/\partial x*||(\partial f/\partial x)^{-1}*\partial f/\partial \dot{x}||^2*||\partial f/\partial y||*w^2}{1-w*||(\partial f/\partial x)^{-1}*\partial f/\partial \dot{x}||} \qquad (9)$$

Increasing of dynamical accuracy is connected in this case with saving one or more internal nodes. It can be mentioned that generation of dynamical MM is carried out in this case by the techniques of statical calculation. The macromodeling approach doesn't depend on input signal form, i.e. the problem of choice of test input signal is excluded.

The proposed methodology can be illustrated by simple examples. Equation (8) allows to construct MM by combination of analytical transformations and numerical calculations. Fig.2 shows the example of MOS subcircuit including serially connected transistors. The purpose consists of calculation the terminal capacitances equations for MM of this subcircuit as multiterminal circuit. For this goal we need the matrices of initial complete model, which are included in equation (8):

$$\begin{array}{cc} \partial f/\partial x & \partial f/\partial y \\ \left|\begin{array}{cc|cc} G_{D2}-G_{S1} & -G_{D1} & -G_{g1} & G_{g2} \\ G_{S1} & G_{D1} & G_{g1} & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{array}\right| & \end{array} \qquad \begin{array}{cc} \partial f/\partial \dot{x} & \partial f/\partial \dot{y} \\ \left|\begin{array}{cc|cc} C_{gS1}+C_{gD2} & 0 & -C_{gS1} & -C_{gS2} \\ 0 & C_{gS1} & -C_{gD1} & 0 \\ -C_{gS1} & -C_{gS1} & C_{gS1}+C_{gD1} & 0 \\ -C_{gS2} & 0 & 0 & C_{gS2}+C_{gD2} \end{array}\right| & \end{array}$$

$$\begin{array}{cc} \partial h/\partial x & \partial h/\partial y \end{array} \qquad \begin{array}{cc} \partial h/\partial \dot{x} & \partial h/\partial \dot{y} \end{array}$$

where G_D, G_S, G_g - MOS model conductances values, C_{gD}, C_{gS} - its capacitances. These means are the nonlinear regime functions. We can get analytical equation for $C_{EQ1,1}$ for condition U_D=0:

$$C_{EQ1,1}(U_{g1},U_{g2},U_D=0) = C_{gD1} + (C_1+C_{gS1}+C_{gS2})*\left(\frac{U_{g1}-V_{T0}}{U_{g1}-U_{g2}-2V_{T0}}\right)^2$$

where V_{T0} - threshold voltage. Fig.2 shows the possibility of the following using the piece-wise approximation for the dependency of V_D. The practical application of digital CMOS MM in LSI simulation provided speed up by 2.5-4 times. The errors in determination the output waveforms are limited by 10 - 15%.

The proposed approach allows to preserve initial

parameters of the complete model. This possibility may be demonstrated by an example of stable current source (fig.3,a). The construction of analog master chip allows to vary the values of resistors. In particular for example in fig. 3,a we can vary value of R_1. The results of numerical calculation are shown in fig.3,b. The characteristics were calculated with the help of formulae (8) for different means of U_1, U_2 and R_1. After approximation of these characteristics as a function of three variables we can get two-terminal MM with saving parameter R_1.

3 The application of special functions for description of model characteristics

The description of physical processes by power (in particular, by linear) and exponential functions is widespread in the semiconductor devices theory. The i-v characteristic of diode with base resistance (fig.4) is a typical example. The description of such processes usually may lead to solution of an equation of the following type: W = V - A*lnW. Here V - argument, W - function. The solution of this equation with the help of elementary functions is impossible. For such problems the application of special implicit function has been proposed [11]. This function is determined by relation:g(V)=exp(V-g(V)) its curve is given in fig.5.

The solution of above mentioned equation may be written in this case as follows: W = A*g(V/A - lnA).

The equation for diode with resistance RD (fig.4) can be written with the help of g-function in the following form: ID = V_T/RD * Z - I_0 , where Z = g[(U_1 - U_2)/V_T + B], B - constant determined by diode parameters. Equation for the conductance in this case is the following: g_D=(1/RD*Z/(1+Z)).

By analogy the economical zener diode model may be given [11] with the help of g-function.

The implementation of g-function to Ebers-Moll model with ohmic resistances (fig.6) leads to two equations:

$$Z_1 = g(U_{BE}/m_E V_T + B_1 - D_1 Z_2)$$
$$Z_2 = g(U_{BC}/m_C V_T + B_2 - D_2 Z_1)$$

where B_1, B_2, D_1, D_2 - constants determined with an account of initial parameters of transistor model equations. These equations are solved by one of known iterative methods. The convergence is provided in this case due to the peculiarities of g-function and only the number of iterations depends on the choice of technique. Such way of using g-function allows to except internal nodes from initial statical model. It is

possible to implement this function for more complex equivalent circuits of bipolar transistors to improving their computational efficiency.

The proposed technique of using this special function is quite universal and can be implement in different simulation problems. Using g-function in macromodeling is also of interest. So g-function can be used for approximation of MM characteristics in many cases, for example, for a typical curve shown in fig.7. Such approximation has the computational advantages due to g-function features. The approximation of characteristic in fig.7 may be written in the form: $I_{OUT} = A*g(U_{OUT}/D + B)$, where determination of coefficients A, B, D is provided as a rule without difficulties. For given characteristic corresponding output current-voltage curve of TTL-gate one can get analytical description. Simplified circuit of output block for high output level and equivalent circuit are given in fig.8,a and fig.8,b. For the equal characteristic of transistors T_1 and T_2 the application of g-function leads to the following equation [11]:

$I_{OUT} = [2V_T/R_1(1 - \alpha_N)] * g[(E - U_{OUT})/2V_T + B] - I_{E0}$, where V_T, α_N, I_{E0} - device model parameters, B - constant. It can be mentioned that this equation saves the connection with initial parameters of complete circuit.

Implementation of special g-function decreases computational efforts already at the stage of circuit equation formulation. The change of the diode and the resistor by single description with the help of g-function improve time spents by 15%. Analogous procedure for bipolar model decreases computer time from 20 to 50% depending on the job regime. This speed up at the formulation stage is explained by increasing of complete number model queries while the calculation times of exponent and g-function are near. The main saving may be got at the solving stage due to reducing of the dimension of complete circuit models in this case.

4.Conclusion

Two approaches to reducing the complexity of models of devices and subcircuit blocks are introduced in the paper. The technique for MM constructing provides the synthesis of quasi-static models in the form that is suited for circuit simulators. This technique is a formalized procedure for reducing the order of nonlinear differential equations and it creates the conditions for solving the problem of MM automatic-generation.

The technique of implementation of special functions allows to get simplified computational equations of the known device models without any loss of accuracy. Its using

gives the possibility to eliminate internal nodes of statical model and decrease the order of resulting circuit model. The combination of these techniques for device model simplification is perspective. In particular the low-frequency computational version of traditional Ebers-Moll model with series resistances can be obtained. Computational efficiency is determined in this case due to reducing the order of circuit model and excluding sources of small time constants.

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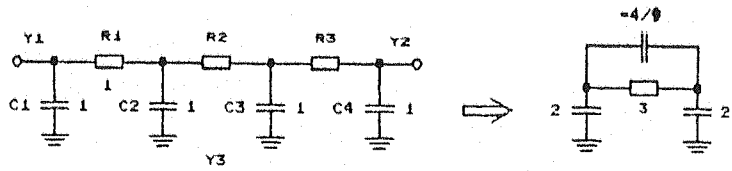

FIGURE 1. RC-NETWORK AND IT'S SIMPLIFIED EQUIVALENT CIRCUIT.

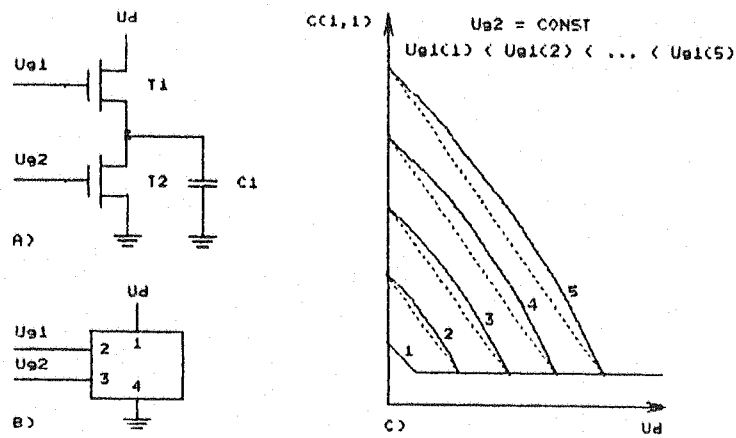

FIGURE 2. CAPACITANCES CHARACTERISTICS (C) OF CMOS-SUBCIRCUIT MACROMODEL (A) IN MULTITERMINAL TYPE (B).

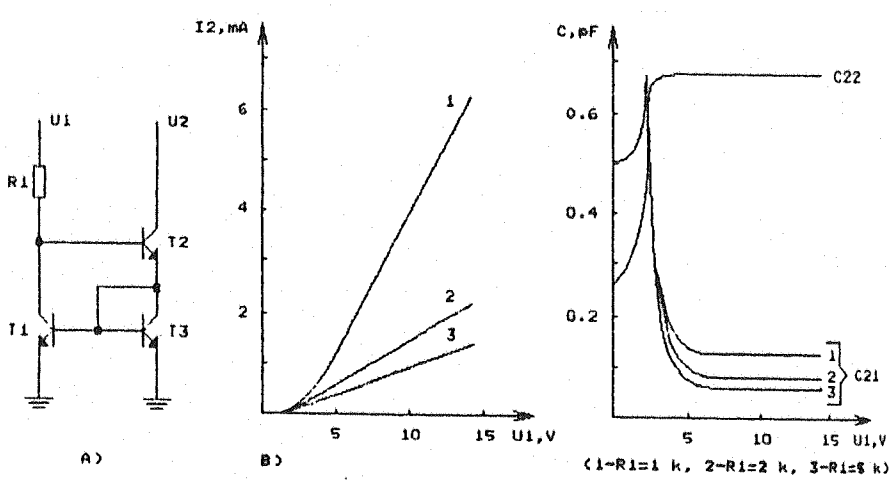

FIGURE 3. THE SCHEME OF STABLE CURRENT GENERATOR (A) AND IT'S MACROMODEL CHARACTERISTICS (B).

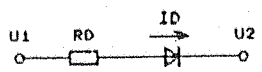

FIGURE 4. EQUIVALENT CIRCUIT OF DIODE WITH RESISTOR.

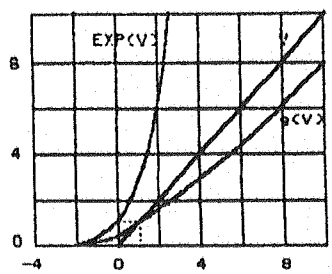

FIGURE 5. g-FUNCTION CURVE.

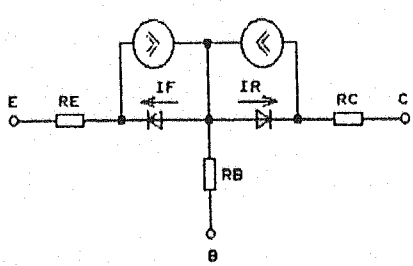

FIGURE 6. EBERS-MOLL MODEL OF BIPOLAR TRANSISTOR WITH OHMIC RESISTANCES.

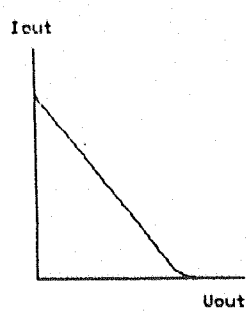

FIGURE 7. EXAMPLE OF MACROMODEL CHARACTERISTIC.

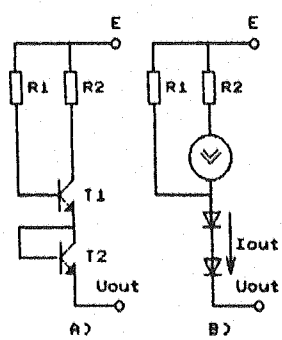

FIGURE 8. OUTPUT STAGE OF TTL-GATE (A) AND IT'S EQUIVALENT CIRCUIT (B).